



# Logic Synthesis Using Synopsys®

By Pran Kurup, Taher Abbasi

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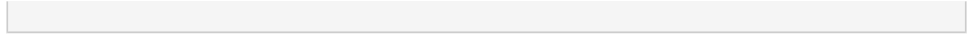
*Logic Synthesis Using Synopsys®*, *Second Edition* is for anyone who hates reading manuals but would still like to learn logic synthesis as practised in the real world. Synopsys *Design Compiler*, the leading synthesis tool in the EDA marketplace, is the primary focus of the book. The contents of this book are specially organized to assist designers accustomed to schematic capture-based design to develop the required expertise to effectively use the Synopsys *Design Compiler*. Over 100 'Classic Scenarios' faced by designers when using the *Design Compiler* have been captured, discussed and solutions provided. These scenarios are based on both personal experiences and actual user queries. A general understanding of the problem-solving techniques provided should help the reader debug similar and more complicated problems. In addition, several examples and dc\_shell scripts (*Design Compiler* scripts) have also been provided.

*Logic Synthesis Using Synopsys®*, *Second Edition* is an updated and revised version of the very successful first edition.

The second edition covers several new and emerging areas, in addition to improvements in the presentation and contents in all chapters from the first edition. With the rapid shrinking of process geometries it is becoming increasingly important that 'physical' phenomenon like clusters and wire loads be considered during the synthesis phase. The increasing demand for FPGAs has warranted a greater focus on FPGA synthesis tools and methodology. Finally, behavioral synthesis, the move to designing at a higher level of abstraction than RTL, is fast becoming a reality. These factors have resulted in the inclusion of separate chapters in the second edition to cover Links to Layout, FPGA Synthesis and Behavioral Synthesis, respectively. *Logic Synthesis Using Synopsys®*, *Second Edition* has been written with the CAD engineer in mind. A clear understanding of the synthesis tool concepts, its capabilities and the related CAD issues will help the CAD engineer formulate an effective synthesis-based ASIC design methodology. The intent is also to assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools.

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### Editorial Review

From the Back Cover

Logic Synthesis Using Synopsys, Second Edition, is for anyone who hates reading manuals but would still like to learn logic synthesis as practiced in the real world. This book should help the reader develop a better understanding of the logic synthesis design flow, optimization strategies using the Design Compiler, test synthesis using the Test Compiler, commonly used interface formats such as EDIF, SDF and PDEF, Links from the Design Compiler to Layout Tools, the FPGA synthesis process, design re-use in a synthesis-based design methodology and a conceptual introduction to behavioral synthesis. Examples in both VHDL and Verilog have been provided throughout the book. Logic Synthesis Using Synopsys, Second Edition covers several new and emerging areas in addition to improvements in the presentation and contents in chapters from the first edition.

### Users Review

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**Rudy Nixon:**

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